Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-12. (Canceled).

13. (Currently amended) A method of assembling an integrated circuit package comprising:

providing a package substrate having a first surface including a first array of interconnection sites and a second array of interconnection sites;

engaging a first integrated circuit die with the package substrate such that an array of interconnection sites on a first surface of the first integrated circuit die are substantially aligned with the second array of interconnection sites of the package substrate;

engaging a second integrated circuit die with the package substrate such that an array of interconnection sites on a first surface of the second integrated circuit die are substantially aligned with the first array of interconnection sites of the package substrate, with the first integrated circuit die positioned amid the package substrate and the second integrated circuit die; and

simultaneously electrically connecting the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die, and the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die,

wherein at least one array of interconnection sites located on the first surface of the substrate remains uncovered by the first and second integrated circuits.

14. (Original) The method of claim 13 wherein the package substrate defines a recessed area that includes the second array of interconnection sites, and

wherein the step of engaging the first integrated circuit die with the package substrate includes:

positioning the first integrated circuit die within the recessed area of the package substrate.

15. (Original) The method of claim 13 wherein the step of simultaneously electrically connecting the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die, and the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die includes:

simultaneously reflowing solder between the first array of interconnection sites and the array of interconnection sites of the second integrated circuit die, and between the second array of interconnection sites and the array of interconnection sites of the first integrated circuit die.

16. (Original) The method of claim 13 wherein the step of engaging the second integrated circuit die with the package substrate includes:

aligning a further array of interconnection sites on the first surface of the second integrated circuit die that is different than the array of interconnection sites on the first surface of the second integrated circuit die with an additional array of interconnection sites on a second surface of the first integrated circuit die that is opposite the first surface of the first integrated circuit die.

17. (Original) The method of claim 16 wherein the package substrate defines a recessed area that includes the second array of interconnection sites, and wherein the step of engaging the second integrated circuit die with the package substrate further includes:

positioning the first integrated circuit die within the recessed area of the package substrate such that the additional array of interconnection sites on the second surface of the first integrated circuit die is substantially aligned with the further array of interconnection sites of the second integrated circuit die.

18. (Original) The method of claim 16 wherein the step of simultaneously electrically connecting the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die, and the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die includes:

simultaneously electrically connecting the further array of interconnection sites of the second integrated circuit die to the additional array of interconnection sites on the second surface of the first integrated circuit die.

19. (Original) The method of claim 18 wherein the step of simultaneously electrically connecting the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die, the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die, and the further array of interconnection sites of the integrated circuit die to the additional array of interconnection sites on the second surface of the first integrated circuit die includes:

simultaneously reflowing solder between the second array of interconnection sites and the array of interconnection sites of the first integrated circuit die, between the first array of interconnection sites and the array of interconnection sites of the second integrated circuit die, and between the further array of interconnection sites of the second integrated circuit die and the additional array of interconnection sites on the second surface of the first integrated circuit die.

20. (Currently amended) A method of assembling an integrated circuit package comprising:

providing a package substrate having a first surface including a first array of interconnection sites and a second array of interconnection sites;

engaging a first integrated circuit die with the package substrate such that an array of interconnection sites on a first surface of the first integrated circuit die are substantially aligned with the second array of interconnection sites of the package substrate;

electrically connecting the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die;

engaging a second integrated circuit die with the package substrate such that an array of interconnection sites on a first surface of the second integrated circuit die are substantially aligned with the first array of interconnection sites of the package substrate, with the first integrated circuit die positioned amid the package substrate and the second integrated circuit die; and

electrically connecting the first array of interconnection sites to the array of interconnection sites of the second integrated circuit die,

wherein at least one array of interconnection sites of the substrate that is concentric with the first and second arrays of interconnection sites remains uncovered by the first and second integrated circuits.

21. (Original) The method of claim 20 wherein the step of electrically connecting the second array of interconnection sites to the array of interconnection sites of the first integrated circuit die includes:

reflowing solder between the second array of interconnection sites and the array of interconnection sites of the first integrated circuit die.

22. (Original) The method of claim 21 wherein the step of electrically connecting the first array of interconnection sites to the array of interconnection sites of the package substrate includes:

reflowing solder between the first array of interconnection sites and the array of interconnection sites of the package substrate.

23. (Original) The method of claim 20 wherein the step of engaging the second integrated circuit die with the package substrate includes:

engaging a further array of interconnection sites on the first surface of the second integrated circuit die that is different than the array of interconnection sites on the first surface of the second integrated circuit die with an additional array of interconnection sites on a second surface of the first integrated circuit die that is opposite the first surface of the first integrated circuit die.

24. (Original) The method of claim 23, and further including:

electrically connecting the further array of interconnection sites of the second integrated circuit die to the additional array of interconnection sites on the second surface of the first integrated circuit die.

25. (Original) The method of claim 24 wherein the step of electrically connecting the further array of interconnection sites of the second integrated circuit die to the additional array of interconnection sites on the second surface of the first integrated circuit die includes:

reflowing solder between the further array of interconnection sites of the second integrated circuit die and the additional array of interconnection sites on the second surface of the first integrated circuit die.

26. (New) A method, comprising:

applying solder to at least one of a first integrated circuit and a second integrated circuit;

tacking the first and second integrated circuits together using solder flux;

inserting the first integrated circuit into a gap of a substrate; and

heating the solder to electrically connect the first integrated circuit and the second integrated circuit.

27. (New) The method of claim 26 wherein heating the solder aligns the first and second integrated circuits.

28. (New) The method of claim 26 wherein the gap of the substrate comprises an opening that extends through the substrate.

29. (New) The method of claim 26 further comprising:

applying solder to at least one of the second integrated circuit and the substrate; and

heating the solder to electrically connect the second integrated circuit and the substrate.

30. (New) The method of claim 29 wherein heating the solder to electrically connect the first integrated circuit and the second integrated circuit and heating the solder to electrically connect the second integrated circuit and the substrate occur simultaneously.

31. (New) The method of claim 26 further comprising applying a hardening material to gaps between at least two of the first integrated circuit, the second integrated circuit and the substrate.

32. (New) The method of claim 29 wherein applying solder to at least one of the first integrated circuit and the second integrated circuit and applying solder to at least one of the second integrated circuit and the substrate comprises applying solder to concentric patterns of interconnection sites.

33. (New) The method of claim 32 wherein the first integrated circuit, the second integrated circuit and the substrate each have at least one concentric pattern of interconnection sites, wherein each concentric pattern has one inner set of interconnection sites and one outer set of interconnection sites that surrounds the inner set.

34. (New) The method of claim 33 wherein at least one concentric pattern of interconnection sites of the substrate remains uncovered by the first and second integrated circuits.